White Paper

Samsung 2bit 3D V-NAND technology

Gain more capacity, speed, endurance and power efficiency

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Traditional NAND technology cannot keep pace with growing data demands

Introduction

Data traffic continues to experience explosive growth worldwide, pushing the limits of NAND flash memory. Inherent limitations in current 2D planar NAND technology prevent capacity expansion due to critical degradation of performance and reliability. Since 2D planar NAND cannot effectively scale capacity with the exponential escalation of data demand, new solutions must be explored.

Samsung 3D vertical-NAND (V-NAND) flash technology offers an innovative solution to satisfy rising data demands. By vertically stacking memory cells in a three-dimensional structure, performance and reliability issues arising from capacity limitations are eliminated, unlocking a new world of 3D memory capabilities. All users, whether end consumers or data centers, can expect smooth, reliable performance at lower costs in a new data-centric world.

Traditional 2D planar NAND technology

A NAND flash chip is composed of memory cells on a plane that enable memory write capabilities. More cells equate to greater memory capacity. Manufacturers strive to shrink cells to fit more cells in less space. In 15 years cell size has gone from 120 nm to 19 nm with 100 times more capacity. Today, cell size has reached 1x nm.

Cell-to-cell interference

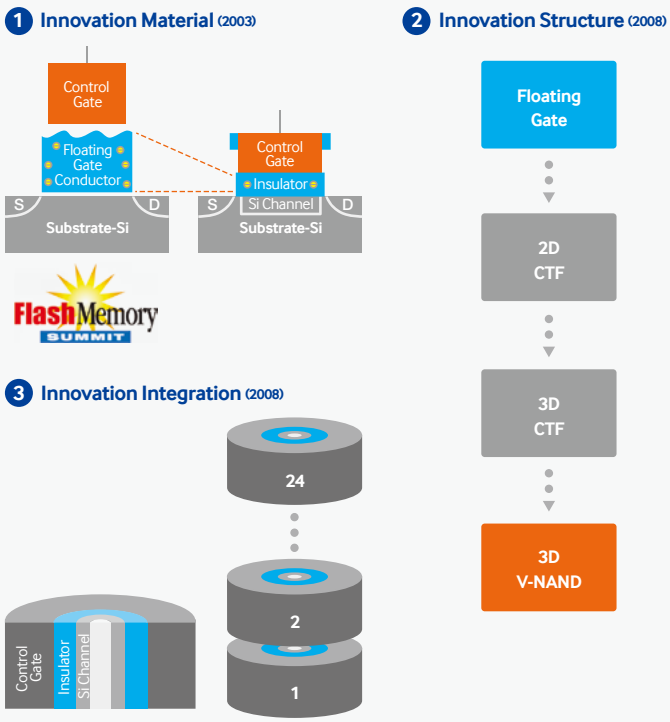
Technical challenges from continued shrinking arise when an electrical charge in a cell flows into an adjacent cell creating cell-to-cell interference, which leads to data corruption. When a cell size goes below 20 nm, the chance for interference drastically increases thereby making it unreliable.

Prohibitive patterning

Patterning is a photolithography process whereby light is used to transfer a geometric pattern from a “mask” to a “photoresist” on the substrate of the chip to create a circuit. With a 1x nm sized cell, light is unable to penetrate the mask. Alternatively, effective shorter wavelength light equipment is cost prohibitive.

Samsung 3D V-NAND memory technology

Samsung’s revolutionary 3D V-NAND technology uses an innovative design that stacks layers of cells on top of one another rather than trying to decrease the cells' length and width to fit into today's smaller form factors. This 3D V-NAND architecture results in higher density using a smaller footprint to eliminate pattern limitations and achieves a much greater scalable capacity to meet current and future data demands.



3D V-NAND’s unique design is made possible by disruptive innovation of material, structure and integration.

Material innovation

Samsung's 3D V-NAND flash memory boasts a cell-to-cell interference-free structure using Charge Trap Flash (CTF) technology. The basis for CTF is a non-conductive layer of silicon nitride (SiN) that temporarily traps electrical charges to maintain cell integrity. This layer has been modified into a three-dimensional form that wraps around the control gate of the cell, acting as an insulator that holds charges, thereby preventing data corruption caused by cell-to-cell interference.

Experience increased capacity with Samsung 3D V-NAND technology

Structural innovation

The vertical integration of 3D V-NAND cell layers requires the use of Channel Hole Technology. This technology allows cells to connect with one another vertically through a cylindrical channel that runs through each column of stacked cells. The 32-layer stacks of cells are connected to over 2 billion channel holes that have been etched from the top layer of the NAND to the bottom. From a top-down view, the entirety of these holes can be seen on a 128 GB NAND chip that is the size a fingernail.

Integration innovation

The cylindrical channels allow layers of cells to be seamlessly integrated vertically. Samsung has achieved greater stacks with the first commercialized 24-layered 3D V-NAND in 2013, with mass production to begin on 32 layers in 2014.

The resulting benefits of 3D V-NAND technology improve memory in several key areas:

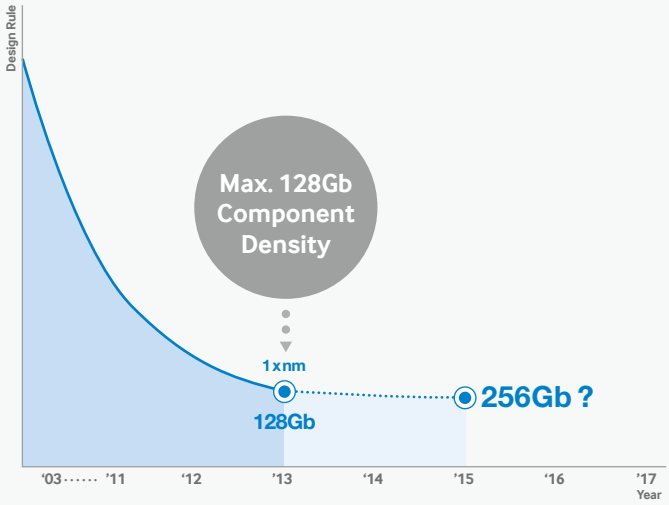
- Capacity for high-quality data
- Speed for faster performance
- Endurance for more traffic
- Efficiency for resource conservation

More layers means more capacity

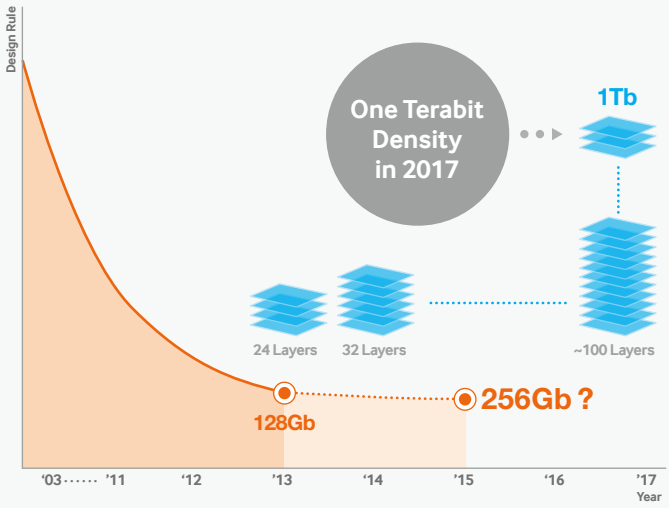
NAND flash capacity is determined by the number of memory cells that can populate a NAND chip, hence, the necessity of cell shrinking to fit more cells into less space. Samsung 3D V-NAND technology offers significantly more capacity by layering cells vertically into three-dimensional stacks, which enables much greater cell density. As a result, professionals and heavy workload users can store and operate data over a longer period of time with greatly improved capacity.

Even with continued cell shrinkage beyond 1x nm, 2D planar NAND design limitations inhibit the ability to go beyond the maximum component density of 128 GB users currently experience. These limitations are due to reliability degradation stemming from cell-to-cell interference and prohibitive patterning. However, the innovative 3D V-NAND design results in a capacity breakthrough that allows up to 100 layers of cells to be stacked with the potential to scale density up to 1 Terabyte (TB) by 2017. As a reference point, the 2D planar NAND density ceiling can only reach the minimum density of 3D V-NAND.

■ 2D Planar NAND Capacity Limitation



■ 3D V-NAND Capacity Breakthrough



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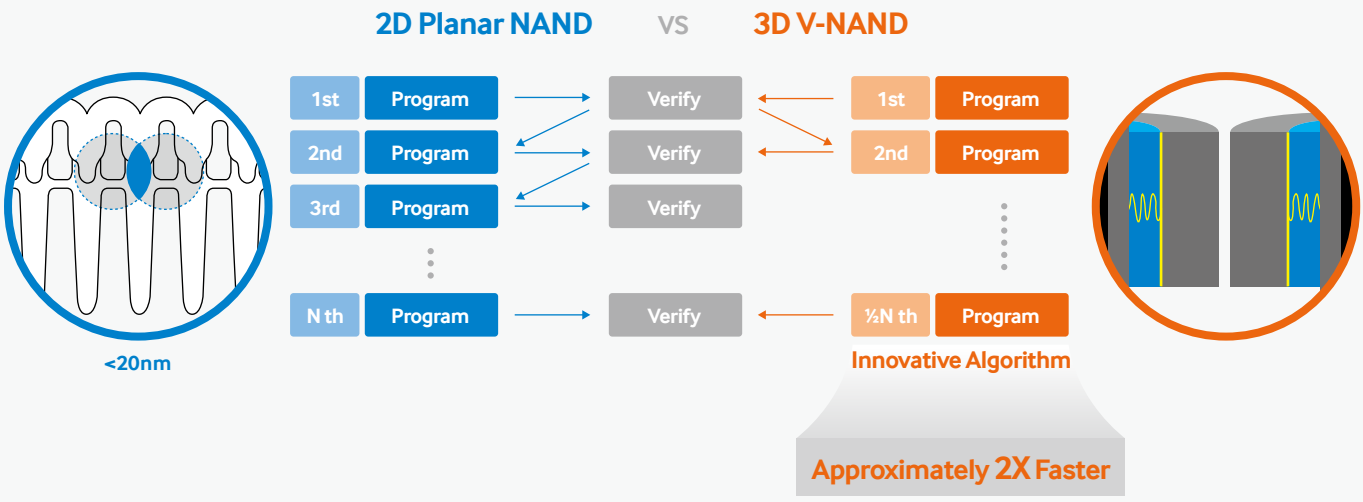
Write data up to twice as fast with unique algorithms

Innovative algorithms means faster performance

NAND flash memory speeds are based on the complexity of the program algorithms that write the data. Traditional 2D planar NAND flash requires the painstaking development of very precise sets of complex program algorithms to prevent data corruption stemming from cell-to-cell interference. Running these highly complex algorithms requires additional time for data to be written, resulting in slower speeds.

Because Samsung 3D V-NAND technology is virtually immune to cell-to-cell interference, due to its CTF technology, it can write data significantly faster. Using distinctive program algorithms, Samsung's 3D V-NAND flash memory can write up to two times faster, resulting in better performance.

Programming Algorithm



Samsung 3D V-NAND delivers superior endurance with improved power efficiency

Less stress means longer use

The endurance of a NAND flash memory chip is decidedly influenced by electric fields produced by cell material and the structure. Higher electric fields place more stress on the chip and, in turn, lower its endurance. The unique materials and structure of 3D V-NAND technology decreases its electric field, which improves its endurance allowing for more data traffic over a longer period of time.

The 2D planar NAND memory cells are partly composed of conductors that allow electrical charges to pass through. The conductors, along with the planar structure, render a relatively higher electric field, which lowers its endurance and diminishes its lifespan. In contrast, 3D V-NAND cells are slightly larger and employ CTF-based insulators allowing it to hold more electrical charges. The material and structural differences of 3D V-NAND help it to produce a lower electrical field, making it more resistant to wear and reducing the risk of cell-to-cell interference. The result is that 3D V-NAND undergoes less stress to deliver more endurance - up to two times that of 2D planar NAND.

Fewer programming steps means less power consumption

To neutralize the ill effects of cell-to-cell interference, traditional 2D planar NAND flash must perform a greater number of programming steps, which is directly correlated to an increase in power consumption. Because Samsung's 3D V-NAND technology has eliminated the issue of interference, the number of programming steps has been vastly reduced. Hence, power consumption is substantially lowered by up to 40 percent.

Increase capacity, speed, endurance and power efficiency

Conclusion

Traditional 2D planar NAND technology has reached the limits of its memory capacity due to structural and material issues evidenced by cell-to-cell interference and prohibitive photolithographic patterning. Samsung 3D V-NAND flash technology overcomes these challenges with its revolutionary vertical, three-dimensional design that insulates individual cells from interference and increases density to eliminate patterning restrictions.

In addition, 3D V-NAND flash innovation offers higher cell density for greater capacity, simplified programming for enhanced speed and power efficiency, and robust materials for more endurance. Samsung 3D V-NAND flash memory is the smart choice for handling today's ever-increasing data demands.

Legal and additional information

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For more information

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Samsung Electronics Co., Ltd.
416, Maetan 3-dong, Yeongtong-gu, Suwon-si, Gyeonggi-do 443-772, Korea

www.samsung.com

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